REMARKS

The following remarks are deemed fully responsive to the office action mailed June 13, 2005. Claims 1 – 22 remain pending, of which claims 1, 5, 11 and 17 are independent.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 5-6, 11, 17-18 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pre-grant Patent Publication Number 2005/00227954 to Rothman (hereinafter "Rothman") in view of U.S. Patent Number 6,618,834 granted to Takeyama (hereinafter "Takeyama"). Respectfully we disagree.

As way of background, the immediate application teaches of computer-aided design ("CAD") systems with reduced memory utilization. The CAD system processes a hierarchical circuit design comprised of blocks. When the CAD system requires access to one of the blocks, it first checks to see if the block to access is already in a circuit model within computer memory. If the block to access is not already within the circuit model, and if adding the block to access to the circuit model would exceed a pre-defined maximum utilization of the computer memory, one or more blocks within the circuit model are unloaded and the block to access is loaded into the circuit model. Blocks are unloaded from the circuit model only when another block needs to be loaded and when loading that block would exceed a pre-defined maximum utilization of the computer memory.

On the other hand, Rothman discloses purging of a file from a non-volatile memory when that file is not accessed within a predetermined period. The purging of the file is based upon a time criteria, not upon a memory usage criteria. Rothman discloses that a file becomes stale if not accessed for X days, where X is one of 7, 30 or 100 days. See Rothman FIG. 2 and paragraph 31. Rothman does not disclose or suggest unloading one or more blocks from memory when attempting to load another block into memory. In fact, Rothman does not disclose or suggest loading of a block into memory at all. Rothman does not disclose management of volatile memory (e.g., dynamic random access memory DRAM) such as used to store programs and data during execution by a processor.

Takeyaman discloses a circuit designing apparatus, timing method and timing distribution apparatus. For example, Takeyaman discloses that "reading out of information regarding a lower hierarchical layer from the circuit information database is unnecessary" and that "the capacity of the working memory and so forth can be saved significantly." See Takeyama col. 9, lines 25-29. Thus, Takeyama saves memory by reducing the need to load information into the memory and certainly not by optimizing the method by which the memory is utilized.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

a) The claimed invention must be considered as a whole;

b) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

c) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

d) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. **Second**, there must be a reasonable expectation of success. **Finally**, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

At the outset, we note that it is not obvious to combine Rothman and Takeyama. The memory management system of Rothman is specifically applied to management of non-volatile memory (e.g., FLASH memory). See Rothman abstract

and at least paragraphs 21-28. This is different from *computer memory* (e.g., computer memory 104, FIG. 2 of the specification), which is typically dynamic random access memory (DRAM) of the type used in a computer to store programs (e.g., CAD tool 114) and data (e.g., circuit model 124) for execution by a processor (e.g., processor 106). As known in the art, non-volatile memory is not used to store programs and data during execution in such computer systems. Therefore it would not be obvious to combine the flash memory management utility of Rothman with the circuit designing apparatus of Takeyama, particularly since the method of Rothman is not suited to DRAM and is not based upon memory usage.

But, even if combined, Rothman and Takeyama do not render claims 1, 5-6, 11, 17-18 and 22 obvious.

Claim 1 recites a method for analyzing a circuit design, comprising:

a) detecting access to at least one block of the circuit design;

b) if the one block is not loaded within a circuit model of computer memory, determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory;

c) if loading the one block into the circuit model would exceed the predefined maximum utilization, unloading one or more blocks from the circuit model and loading the one block into the circuit model;

d) if loading the one block into the circuit model would not exceed the predefined maximum utilization, loading the one block into the circuit model.

As required by step b) of claim 1, neither Rothman nor Takeyama determine whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory if the block is not already loaded in the circuit model. The combination of Rothman and Takeyama also do not disclose unloading one or more blocks from the circuit model and loading the one block into the circuit model if loading the one block into the circuit model would exceed the predefined maximum utilization, as required by step c). The combination of Rothman and Takeyama also does not disclose a predefined maximum utilization of the

memory as required by steps c) and d). As noted above, Rothman does not disclose unloading of blocks based upon a requirement to load a new block into memory. Specifically, Rothman discloses purging of a file to recover storage space if the file has not been accessed within a predetermined period. See Rothman abstract and at least paragraph 31. Therefore, Rothman in view of Takeyama cannot render claim 1 obvious.

Reconsideration of claim 1 is respectfully requested.

Claim 5 recites a system for analyzing a circuit design, including:

a) computer memory for storing a circuit model of the circuit design;

b) an analysis tool for analyzing the circuit design by accessing one or more blocks of the circuit model; and

c) a model manager for (a) loading one or more blocks of the circuit design to the circuit model and (b) unloading one or more blocks from the circuit model such that the circuit model does not exceed a predefined maximum utilization of the computer memory.

Neither Rothman not Takeyama disclose a model manager for loading one or more blocks of the circuit design to the circuit model and unloading one or more blocks from the circuit design such that the circuit model does not exceed a predefined maximum utilization of the computer memory, as required by element c) of claim 5. As argued above, neither Rothman not Takeyama disclose a predefined maximum utilization of the computer memory.

Claim 6 depends from claim 5 and therefore benefits from like argument.

For at least these reasons, Rothman and Takeyama cannot render claims 5 and 6 obvious. Reconsideration of claims 5 and 6 is respectfully requested.

Claim 11 recites a system for analyzing a circuit design, including:

a) means for detecting access to at least one block of the circuit design;

b) means for determining whether loading the one block into a circuit model, stored within computer memory, would exceed a predefined maximum utilization of the computer memory when the one block is not currently within the circuit model;

c) means for unloading one or more blocks from the circuit model and loading the one block into the circuit model when loading the one block into computer memory would exceed the predefined maximum utilization; and

d) means for loading the one block into the circuit model when loading the one block into the computer model would not exceed the predefined maximum utilization.

As argued above, Rothman does not disclose determining whether loading the one block into a circuit model, stored within computer memory, would exceed a predefined maximum utilization of the computer memory when the one block is not currently within the circuit model, as required by element b) of claim 11. Rothman does not disclose unloading one or more blocks from the circuit model and loading the one block into the circuit model when loading the one block into computer memory would exceed the predefined maximum utilization as required by element c). Rothman does not disclose loading the one block into the circuit model when loading the one block into the computer model would not exceed the predefined maximum utilization as required by element d). Moreover the system of Rothman does not operate with computer memory as used by the immediate application. Takeyama does not make up for the shortcomings of Rothman, and therefore, even when combined, Rothman and Takeyama cannot render claim 11 obvious.

Reconsideration of claim 11 is respectfully requested.

Claim 17 recites a software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for analyzing a circuit design with reduced memory utilization, including:

a) instructions for detecting access to at least one block of the circuit design;

b) instructions for recording the access when the one block is loaded within a circuit model of computer memory;

c) instructions for determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the

computer memory, when the one block is not loaded within the circuit model;

d) instructions for unloading one or more blocks from the circuit model and loading the one block into the circuit model, when loading the one block into the circuit model would exceed the predefined maximum utilization; and

e) instructions for loading the one block into the circuit model, when loading the one block into the circuit model would not exceed the predefined maximum utilization.

As argued above, Rothman does not disclose determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory, when the one block is not loaded within the circuit model, as required by element c) of claim 17. Rothman also does not disclose unloading one or more blocks from the circuit model and loading the one block into the circuit model, when loading the one block into the circuit model would exceed the predefined maximum utilization as required by element d). Again, Rothman does not disclose loading the one block into the circuit model, when loading the one block into the circuit model would not exceed the predefined maximum utilization as required by element e). Further, Takeyama does not overcome the shortcomings of Rothman and therefore, even when combined, Rothman and Takeyama do not render claim 17 obvious.

Reconsideration of claim 17 is respectfully requested.

Claims 18 and 22 depend from claim 17 and benefit from like argument. However, these claims have additional features that patentable distinguish over Rothman in view of Takeyama. For example, claim 18 further recites instructions for recording the access in a block access table and claim 22 recites setting the predefined maximum utilization. As argued above Rothman does not disclose a predefined maximum unitization for the computer memory, let alone setting the predefined maximum utilization. Takeyama has no relevant disclosure to teach these claims either.

Thus Rothman in view of Takeyama cannot render claims 18 and 22 obvious. Reconsideration of claims 17, 18 and 22 is respectfully requested.

Claims 2-4, 7-10, 12-16 and 19-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rothman in view of Takeyama in further view of in view of U.S. Patent Number 6,256,711 granted to Berliner (hereinafter "Berliner"). Respectfully we disagree.

Berliner discloses a method for purging unused data from a cache memory. Berliner discloses that the method is "particularly applicable to cache memories established on rotating magnetic media." See Berliner col. 4, lines 40-41. Berliner continues, "when all sub-blocks within the cache memory have been filled, sophisticated, system resource-intensive algorithms **are not** employed to determine which is the oldest or the least frequently used sub-block of data. Instead, sub-blocks of data are removed in a pseudo-random manner until ample space is made within the cache." See Berliner col. 4, lines 44-49 (*Emphasis added).* Berliner does not teach of determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory as required by independent claims 1, 5, 11 and 17; therefore Berliner does not make up for the shortcomings of Rothman and Takeyama as described hereinabove.

Thus when combined, Rothman, Takeyama and Berliner do not render independent claims 1, 5, 11 and 17 obvious. For at least this reason, claims 2-4, 7-10, 12-16 and 19-21 also are not rendered obvious by Rothman in view of Takeyama and in further view of Berliner.

Claims 2-4, 7-10, 12-16 and 19-21 have additional features that patentably distinguish over Rothman, Takeyama and Berliner. For example, claim 2 recites updating a block access table to record the access to the one block, if the one block is loaded within the circuit model; wherein the steps of updating and loading comprise recording the access to the block in the block access table; and wherein the step of unloading comprises utilizing the block access table to determine which blocks to unload from the circuit model. Neither Rothman, Takeyama nor Berliner disclose using a block access table. Claim 3 recites utilizing an LRU caching technique with information of the block access table to determine which blocks to unload. Neither Rothman, Takeyama nor Berliner discloses utilizing an LRU caching technique or a

block access table. Claim 4 recites utilizing an LFU caching technique with information of the block access table to determine which blocks to unload. Neither Rothman, Takeyama nor Berliner disclose utilizing an LFU caching technique or a block access table for determining which blocks to unload.

Claims 7-10 depend from claim 5 and benefit from the above arguments for claim 5. Further, claim 7 recites a block access table for recording access to blocks of the circuit model by the analysis tool; claim 8 recites the model manager being operable to determine which blocks to remove from the circuit model by utilizing information of the block access table; claim 9 recites the model manager employing an LRU caching technique with information of the block access table to determine which blocks to remove from the circuit model; and claim 10 recites the model manager employing an LFU caching technique with information of the block access table to determine which blocks to remove from the circuit model. As argued above, Neither Rothman, Takeyama nor Berliner disclose utilizing an LFU caching technique or a block access table for determining which blocks to unload.

Claims 12-16 depend from claim 11. Claim 12 recites means for recording the block access; claim 13 recites wherein the means for recording records the block access in a block access table; claim 14 recites means for utilizing the block access table to determine which blocks to unload from the circuit model; claim 15 recites means for utilizing an LRU caching technique to determine which blocks to unload from the circuit model; and claim 16 recites means for utilizing an LFU caching technique to determine which blocks to unload from the circuit model. As argued above, Neither Rothman, Takeyama nor Berliner disclose utilizing an LFU caching technique or a block access table for determining which blocks to unload.

Claims 19-21 depend from claim 17. Claim 19 recites instructions for utilizing the block access table to determine which blocks to unload; claim 20 recites instructions for utilizing an LRU caching technique to determine which blocks to unload; and claim 21 recites instructions for utilizing an LFU caching technique to determine which blocks to unload. As argued above, Neither Rothman, Takeyama nor Berliner disclose utilizing an LFU caching technique or a block access table for determining which blocks to unload.

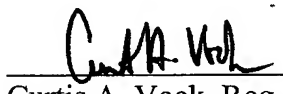
Contrary to the Examiner's assertion, Berliner provides no information on use of a block access table, LRU and LFU caching techniques. In fact, as noted above, Berliner specifically teaches away from use of tables and LRU and LFU techniques. For example, in step 5 of FIG. 2, Berliner discloses scanning "the hierarchical structure of cached sub-blocks without regard to age or frequency of use in order to locate in a pseudo-random manner a sub-block that is not currently being accesses by an application." See Berliner col. 5 line 66 through col. 6 line 2.

The combination of Rothman, Takeyama and Berliner cannot render claims 2-4, 7-10, 12-16 and 19-21 obvious. Reconsideration of claims 2-4, 7-10, 12-16 and 19-21 is respectfully requested.

Applicant has addressed all rejections of the pending office action and requests reconsideration and allowance of all claims.

Applicant believes no fees are due in connection with this response; however, if any fee is deemed necessary, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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